MMC
(Modular Multilevel Converter)

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1. General information

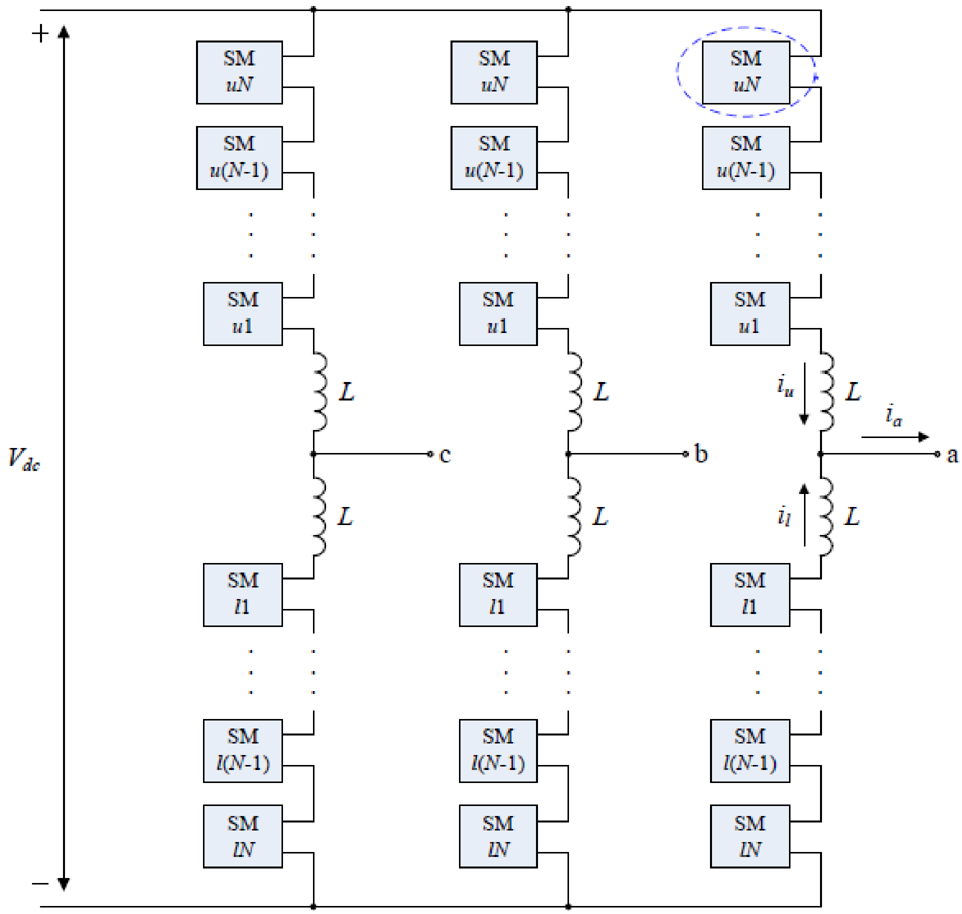
1 – General information

- Project general objective
  - To develop a **scaled MMC-based test-rig** to provide a facility for research and development of **control algorithms for VSC-HVDC** multi-terminal links and meshed grids.
- Supply from TECNALIA to UNSW (University of New South Wales) Australia. 2015.

1 – General information

- Why MMCs for HVDC technology?
  - Real VSC converters at HVDC substations: around 1GW and +/-320kV.
  - Constraints of semiconductors:
    - Imax of IGBTs around 3kA
    - Necessary high V to reach 1GW
    - Vmax of IGBTs around 6,5kV
  - MMC topology is able to reach very high power using actual semiconductors with hundreds of sub-modules. It is very flexible.
  - The solutions of the main manufacturers are based this topology

Modular Multilevel Converters



- Cascaded connection of sub-modules to achieve high voltage levels.
- Sub-modules are connected in series creating arms.
- Each phase leg comprises two arms (upper and lower arms).
- It is structurally scalable and can theoretically meet any voltage level. Thus, it is very well suited for HVDC applications.

Main characteristics

- Composed by 96 power sub-modules

- Configurable as:
  - a 3-phase MMC converter unit with 96 power sub-modules (16 SM per arm)
  - two independent 3-phase MMC units, each one with 48 sub-modules (8 SM per arm), that can be connected following a point-to-point VSC-HVDC scheme or
  - up to 4 independent 3-phase MMCs, each one with 24 sub-modules (4 SM per arm), to analyze multiterminal links and meshed VSC-HVDC

- Nominal power of 40 kW at a DC voltage level of 1600V

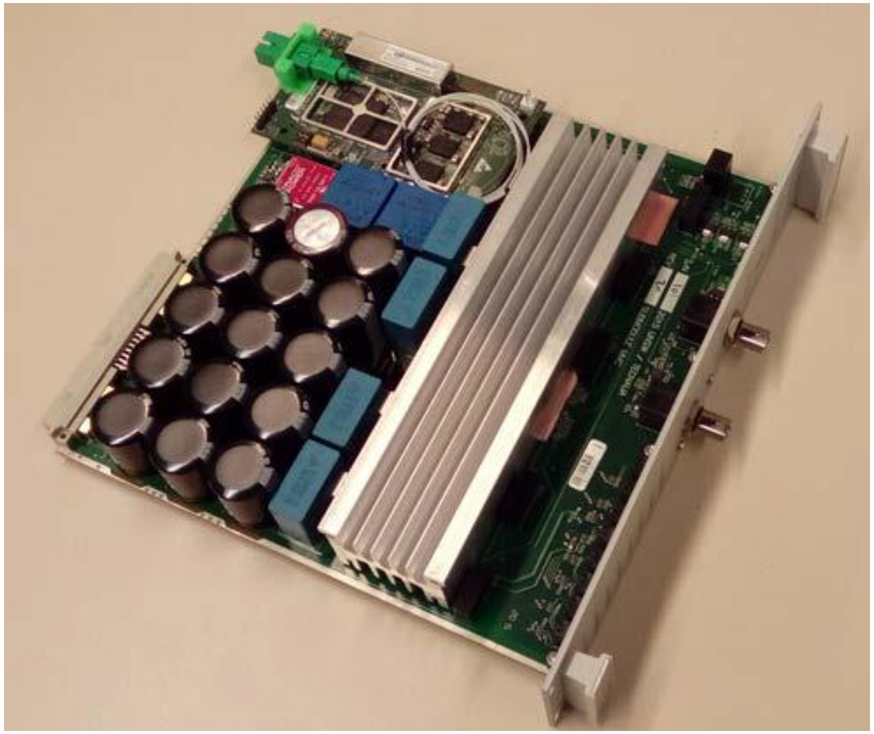
- Central Control at dSpace

1 – General information

Tecnalia MMC Test System

2. Power sub-modules

- Main characteristics
  - 4 MOSFETs per sub-module
  - Half-bridge or full-bridge configuration
  - Configurable DC-bus to emulate different capacitances

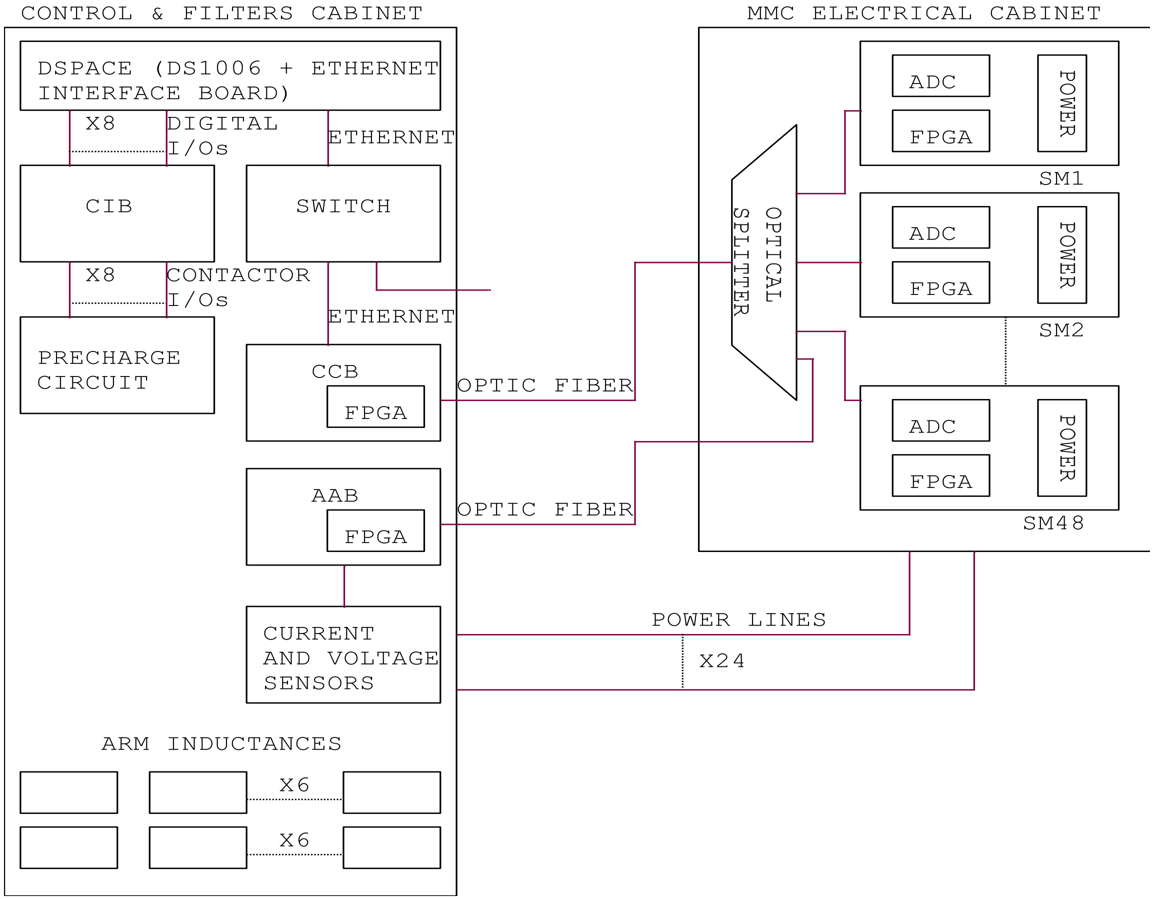


Test-Rig Power Sub-Module

3. Control system

- Objective
  - To develop a control architecture **able to control converters with hundreds of sub-modules** as in a **real MMC converter** and working synchronously. In addition, it features the following characteristics:
    - High reliability
    - Reduced wiring to allow easy installation and maintenance
    - Highly scalability to fit with converters with different number of cells

3 – Control system

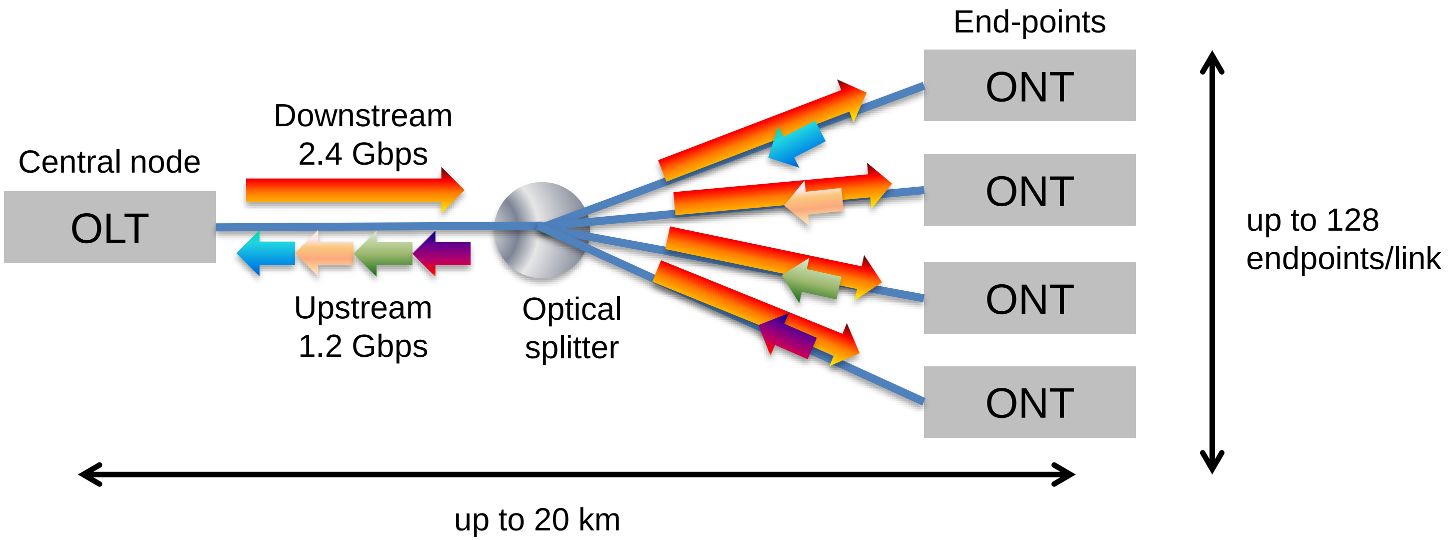


System Diagram

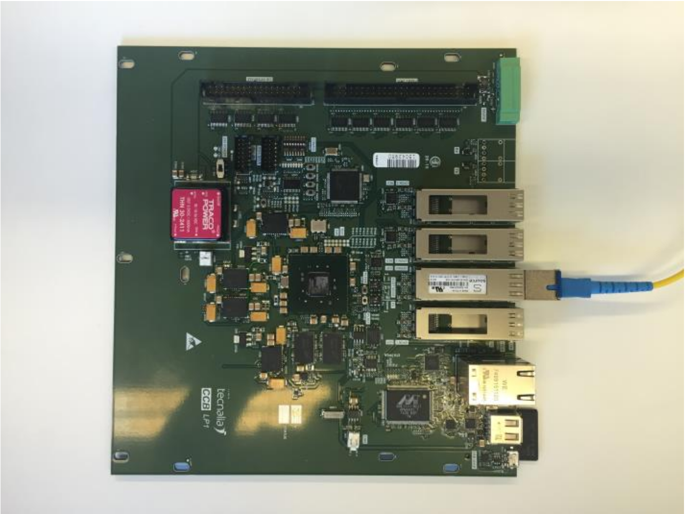
3 – Control system

- Characteristics:
  - Distributed digital controller
  - Each **sub-module houses an FPGA** that generates the driving signals of the MOSFETs and manages the communication with a central control unit (CCU)
  - A single fiber optical cable runs between each sub-module and an optical hub
  - The CCU is also connected to the optical hub using a single fiber optical cable
  - Additional cable for **redundancy** to failures

Passive Optical Networks (PON). Monitoring and Control Communication System



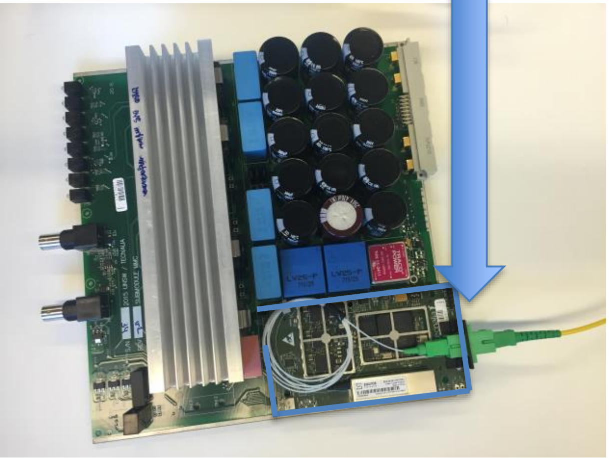
- **Point to Multipoint** optical to the end-point network
- **Passive** (unpowered) distribution network using splitters
- A **single fiber** serves up to **128 end-points**
- **Donwstream** signals are **broadcast @ 2.4Gbps**
- **Upstream** signals are multiplexed and **combined** (TDMA) @1.2Gbps
- Extensively used in access networks (FTTH)



Xilinx® Zynq® based CCU

Xilinx® Artix-7® based end-point.
Plugable

Measurement board



Submodule

3 – Control system

- The **CCU receives** the DC voltage of the sub-modules, the arm currents, the DC and AC voltage **measurements** and the converter **alarms** through the communication network in each modulation period
- The **CCU executes the modulation strategy** and the **high level control algorithms**
- The **outputs of CCU** are the **duty cycles** that are send back to the sub-modules
- It is possible to communicate between the CCU and real time fast prototyping hardware (**dSPACE**, Opal RT, or National Instruments)
- Control algorithms can be split between the CCU and the real time hardware
- Implementation of the control algorithms using Matlab-Simulink. Fast prototyping and testing of the developed controllers

4. Status and next steps

4 - Status and next steps

- Actual status:
  - **Successfully commissioned** and installed in the power electronic laboratory of the UNSW. Currently, UNSW researchers are using it to investigate VSC-HVDC links
- Next steps:
  - Development of control algorithms for meshed HVDC grids
  - Research on novel circulating current controllers with improved characteristics under grid unbalances
  - Benchmarking of different circulating current controllers
  - Experimental assessment of harmonic stability studies
  - The multilevel converter can also be configured as a cascaded H-bridge converter allowing its use not only as a test bench for HVDC systems but also for other applications such as MV-STATCOMs or large PV applications

5. Barriers to innovation deployment

5 - Barriers to innovation deployment

- Very complex systems
- Very expensive systems
  - Difficult to increase the power in demonstrators
- Technology well controlled by a few manufacturers. As they want to protect their technology:
  - Difficult to work with them
  - Few information for the utilities
- Legal framework: not very developed, but working on it

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